Tom Mayo

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Objective

Business leader in industrial communications systems

Summary

- 26 years of professional computer hardware and software engineering experience.
- 10 years technical leadership training and experience.
- Master's degree in electrical engineering.
- Analysis and synthesis skills drawing on experience in several electrical engineering disciplines.
- Strength working with customers to turn needs into requirements and develop products to meet them.
- Experience estimating development costs and schedules and tracking projects to completion.
- Computer-aided logic design experience, focusing on VHDL.
- Radio frequency design and construction exposure through Amateur Radio and professional experience.
- Diverse experience with computer tools and platforms.

Work Experience

GE MDS, LLC; Rochester, NY **5/97 to Present**

Leadership Roles as a Project Manager

Project Manager for wireless system design and deployment services. Preparing and presenting customer proposals. Leading team of five people in multiple concurrent projects. Responsible for schedules up to 18 months, budgets up to $1MM plus. Maintaining profitable and successful projects. Responsibilities include supervising and advising technical design of data radio communications systems design and analysis.

Project Manager for wireless data communications product development for the railroad industry. Applications include Remote Control Locomotive, Train Control, and Distributed Power. Responsible for customer interfacing, requirements definition, schedule coordination, budget tracking, outsourcing and on-site representation. Managed the technical team to meet product requirements, system architecture, and schedule needs. Coordinated production and manufacturing documentation, product assurance, and follow-on customer support.

Other Leadership Roles

Project Lead for a TCP/IP proxy platform providing network access to industrial radio diagnostics and data. Led a 4-member team. Performed project planning and tracking, requirements and product assurance coordination, training, and production and manufacturing support.

Project Lead for a 106 kbps 900 MHz Frequency Hopping Spread Spectrum radio product family. Led a 10-member team. Performed project planning and tracking, requirements definition, and oversight of product assurance function. Interfaced to multiple customers for training and support needs and follow-on system requirements definition. Responsible for the hardware design for a 65 MHz PowerPC MPC850 board with USB, Ethernet, memory and multiple serial interfaces.

FPGA Team Lead for a 256 to 1024 kbps frequency hopping spread spectrum radio modem. Implemented and co-designed a 2- and 4- level FSK modem in a Xilinx FPGA including mean removal, timing recovery, shaping and equalization, adaption, frame detection, scrambling and descrambling, and data delivery. Digital Hardware Designer for a radio board, performing architecture design and component selection for PowerPC MPC850 CPU, Xilinx Spartan 2 FPGA, memory, and Ethernet interface.

Design Roles as a Senior Development Engineer

Responsible for digital design and overall board design coordination for a 900 MHz 64 kbps to 768 kbps data radio. Responsibilities include architecture design and component selection for PowerPC MPC850 CPU, memory, Ethernet, and EIA-530 interface. Other responsibilities include QAM modem analysis and configuration, DSP processor and memory hardware design, coordination of schematic capture and board layout and routing, production support, and FPGA design assistance.

Responsible for overall board and hardware product design of a Terminal Server/Network Proxy product. Included architecture design and component selection of PowerPC MPC860 CPU, memory, Ethernet and EIA-232 interfaces. Also included writing C and Assembly firmware for pSOS board support package. Saw product through from conception to production.

General Dynamics Defense Systems, Pittsfield, MA 10/94 to 5/97
Senior Digital Design Engineer

Participated in candidate interviewing and selection for the Edision Engineering technical leadership program.

Member of an IR&D team developing a low cost two-axis machine gun stabilization system. Performed requirements definition, product design, and component selection. Responsible for microcontroller selection and architecture design. Also responsible for three Altera PLD designs in VHDL and real time firmware development in C. Firmware development included design of a task switching real time OS and two 512 Hz control loops. Performed field integration and test of overall system.

Designed and implemented discrete I/O controls, a VME slave interface, and a catastrophic error monitor in a 16 MHz Actel 1280 FPGA. Assumed follow-on responsibility for a VME discrete I/O circuit card which includes 16 solid-state relay outputs and 28 opto-coupled inputs, and the above mentioned FPGA. This responsibility includes supporting software development and production.

Assumed design responsibility for four 6 MHz Actel 1280 FPGAs including timing, serial communication, DMA I/O, and charge injection device camera timing controller designs. Performed redesign of CID controller FPGA entirely using VHDL. Assumed follow-on responsibility for two circuit cards for an inertial measurement system. These responsibilities include making several design modifications to support feature enhancements.

Used VHDL to design several 3 MHz Altera 5032 PLDs for use in test circuits.

Lockheed Martin Defense Systems, Pittsfield, MA 6/92 to 10/94
Edison Engineering Program Engineer

Rotated to three assignments including Systems Analysis, Analog Circuit Design, and Digital ASIC and Module Design. Developed processor and network resource models in C for FDDI network simulation. Designed and implemented analog circuit for detection of

Ring Laser Gyro extinction. Developed several functions implemented in Actel 1280 FPGAs.

General Electric Ordnance Systems, Pittsfield, MA **1/91 to 8/91**
Engineering Co-op, Embedded Software

Updated Motorola 68000 C firmware for accelerometer test station. Included real-time operating system interface, display driver, and signal processing code.

Developed menued test sequence control application in C with Unix, X-Windows, and TCP/IP components.

Pratt & Whitney, East Hartford, CT **6/90 to 1/91**
Engineering Coop, Development Operations

Developed a multi-platform UNIX socket-based NC file server system for distributing and archiving NC programs for use in a TCP/IP networked machine shop. Responsibilities included design and implementation of a Curses-based menu system.

Bradley Ward, Inc., Atlanta, GA **5/89 to 8/89**
Intern, Software Engineering

Updated and rewrote on-line documentation for Process Monitoring and Information System (PMIS) software configuration and user-interface applications. Independently developed data base browsing utility eventually incorporated into the company's tool suite.

General Foods, Tarrytown, NY **8/87 to 8/88**
Engineering Coop, Computer Process Control Group

Installed and integrated PMIS software with Allen Bradley and Foxboro process control hardware to monitor and control a 17-story coffee decaffeination process at the Maxwell House plant in Houston, TX. This project involved writing many algorithms in FORTRAN for incorporation into the PMIS runtime application.

Computer Experience

Operating Systems: Linux, MS-Windows, DOS, some pSOS.
Languages: Tcl/Tk, Python, VHDL, C, C++, HTML, some PHP, Java, Forth, and Assembly.
Platforms: PC, Raspberry Pi, Embedded PowerPC, some HC11 and 68K.
Tools: Simpy, ActiveVHDL, Synplify, Xilinx ISE, Viewlogic, Matlab, MS Office, MS Project.

Education

Rensselaer Polytechnic Institute **8/95**
Master of Engineering, Electrical Engineering
GPA: 3.375/4.0

Thesis: Converting State Diagrams into Synthesizable VHDL, Dr. Kenneth Rose, Adviser
Concentration: Communication Systems and Information Processing.
Course work: Stochastic Signals and Systems, Intro. to Digital Communication, Digital Communication Engineering, Advanced DSP, Pattern Recognition, Advanced VLSI Design.

University of Massachusetts, Amherst **5/92**
Bachelor of Science, Electrical Engineering
GPA: 3.882/4.0

Senior Electives: Communication Systems, Digital Signal Processing, Control Systems.

Awards and Honors

Richard V. Monopoli Scholarship award for excellence in controls, University of Massachusetts, Amherst, 1992.
Eta Kappa Nu electrical engineering honor society, University of Massachusetts, Amherst, 1991-1993.
Tau Beta Pi engineering honor society, University of Massachusetts, Amherst, 1991-1993.

Hobbies and Interests

Academic: Teach yearly communications system design class at GE for students across many GE sites. Taught two in-plant courses yearly at Lockheed Martin Defense Systems: Mathcad and Fourier Analysis. Taught a C++ Class in April 1997 at Berkshire Community College
Amateur Radio: Hold Amateur Extra Class license, callsign N1MU. Founded the Microwave Data Systems Amateur Radio Club, K2MDS. Design, construct, and operate portable microwave radio stations, including equipment from 50 MHz to 5 GHz. Authored an article in Microwave Projects, a book published by the Radio Society of Great Britain. Published two articles in the Rochester VHF Group Journal.
Computer: Administer 2ub.org web site and domain. Maintain a TCP/IP Linux and Windows network and home automation system at home. Design and write RoverLog Amateur radio contest logging software in Tcl/Tk, used by many Amateur Radio operators.

For references, please contact me at tmayo6@gmail.com.